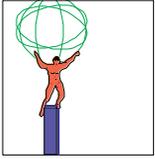


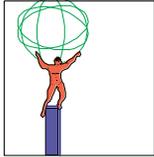
U.S. ATLAS



WBS 1.1 Silicon Subsystem

M. G. D. Gilchriese
(LBNL)

U.S. ATLAS



WBS 1.1 Institutions

SUNY Albany

Iowa State University(new since last review)

UC Berkeley/LBNL

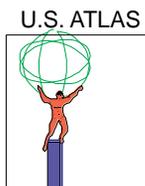
University of New Mexico

Ohio State University

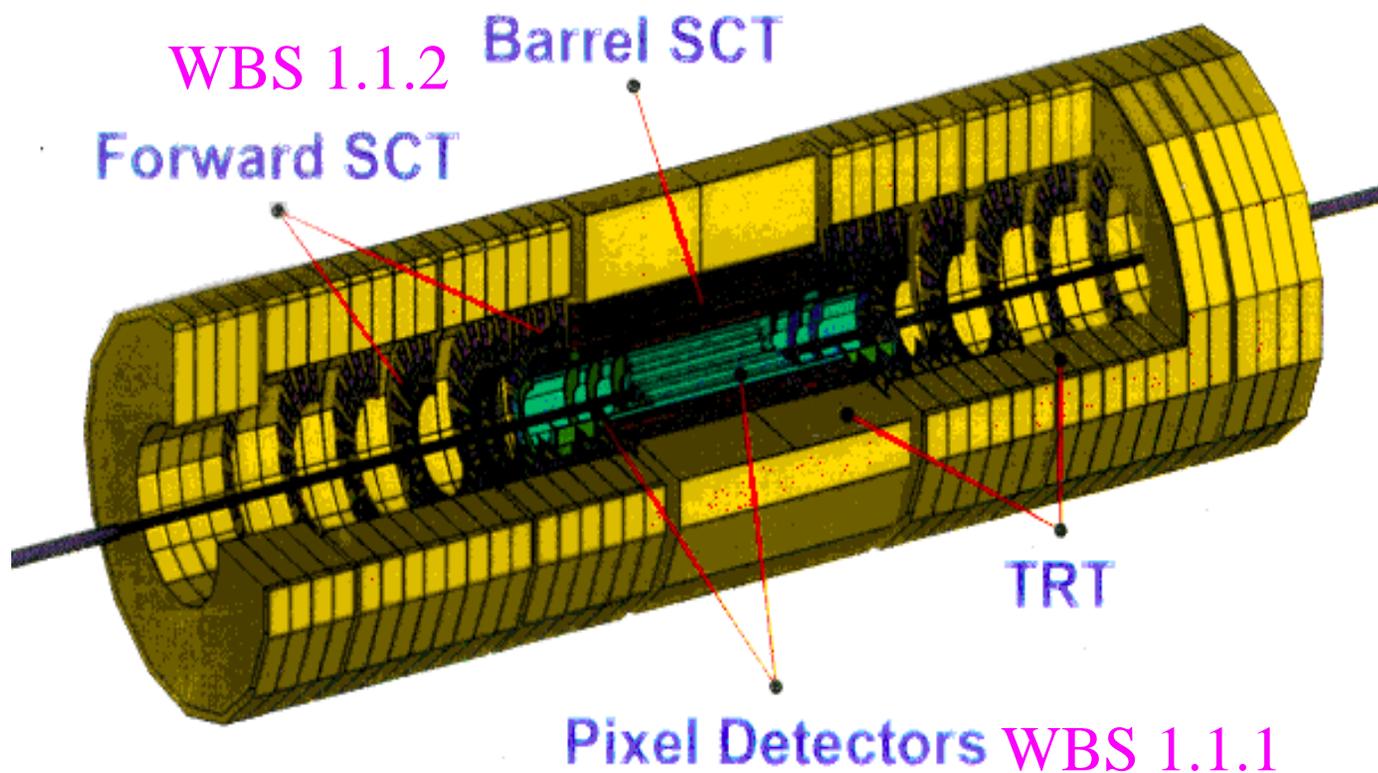
University of Oklahoma/Langston Univ.

UC Santa Cruz

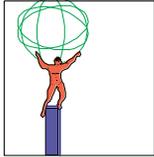
University of Wisconsin



Silicon Subsystem

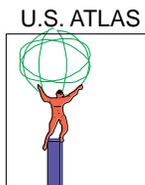


ReadOut Drivers - WBS 1.1.3



WBS 1.1.3 Read-Out Drivers

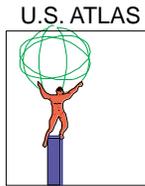
- **RODs: off-detector VME boards that receive/transmit signals from/to all pixel and SCT modules.**
- **Baseline plan: preprototype->prototype->production model->production**
 - ◆ Design team unable to converge on common technical solution for preprototype
 - ◆ Review held end-March 99 to make selection
 - ◆ Design team changed. Irvine left. Iowa State joined. Lost time.
- **Current plan: prototype -> production model ->production(in stages) - see milestones next page. Increased scope of prototype.**
- **Design review of status of prototype held on Dec. 17. Design advancing well, follow up review scheduled just before submission for fabrication.**
- **Scope**
 - ◆ The number of RODs estimated to be needed for pixels and SCT is now much better understood compared to FY97 baseline estimate, and has gone down substantially.
 - ◆ SCT RODs were US(75%)-UK(25%) deliverables. Pixel RODs were 100% US. Compared to baseline design assumptions from 1997, design has changed to (a) eliminate ASICs from UK and (b) shift all responsibility for optical receivers/drivers (Back-of-Crate Card) and Timing Interface Module to UK. Interface with US deliverable now much cleaner.
 - ◆ ETC now includes fabrication of 100% of both pixel and SCT RODs.



WBS 1.1.3 ETC

- WBS structure changed substantially.
- Completely revised estimates for labor and fabrication made for ETC.
- Fabrication costs detailed by type of ROD. Although all have same basic design, pixels are different than SCT, differences within pixels(B-layer vs outer layers), etc
- Some aspects of division of testing between US and Europe still to be sorted out.

				TPC	
	Baseline	ETC	Actuals	ETC+Actuals	Delta
WBS	FY00 \$K	FY00\$K	\$K	\$K	\$K
1.1.3	2551	2068	630	2698	(147)



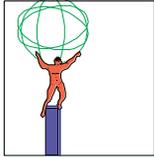
WBS 1.1.3 Risks and Issues

- **Risks**

- ◆ Continuity of design team -> go as fast as possible
- ◆ Interfaces not under US control changed -> working hard to avoid this. Have good communication with UK and pixel/SCT electronics coordinators. Need to address also interface with ROB.
- ◆ Intrinsic board complexity(SCT has 96 links) -> build prototype and see.

- **Issues**

- ◆ Relative role of US and UK in production testing of SCT RODs still to be sorted out. Similar issue will come along for pixels.
- ◆ Long lead-time procurement of critical parts -> after FDR and before PRR according to current schedule.
- ◆ Life-time buy of critical parts and spares not part of baseline. General ATLAS problem but exacerbated here by critical dependence on parts that rapidly will become obsolete.

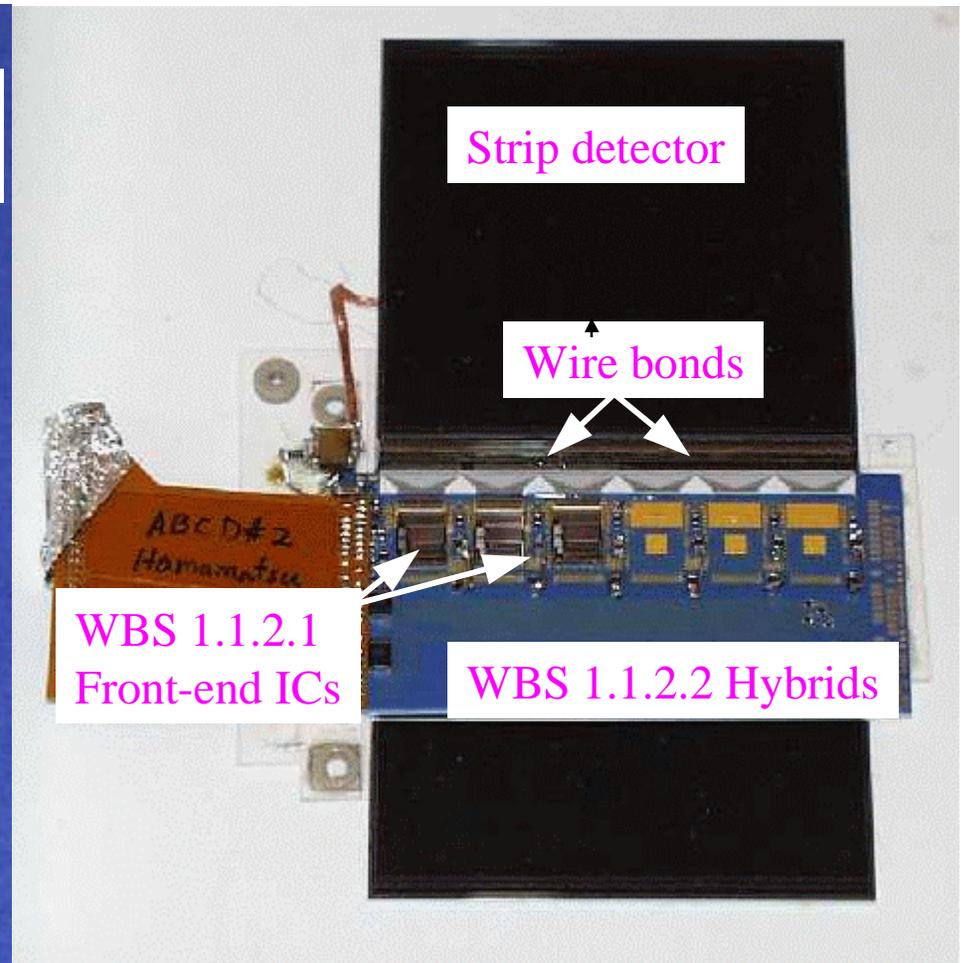


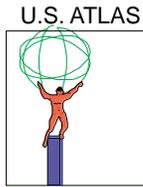
WBS 1.1.2 Silicon Strip System

Double-sided dummy module



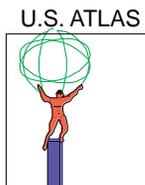
Single-sided active module





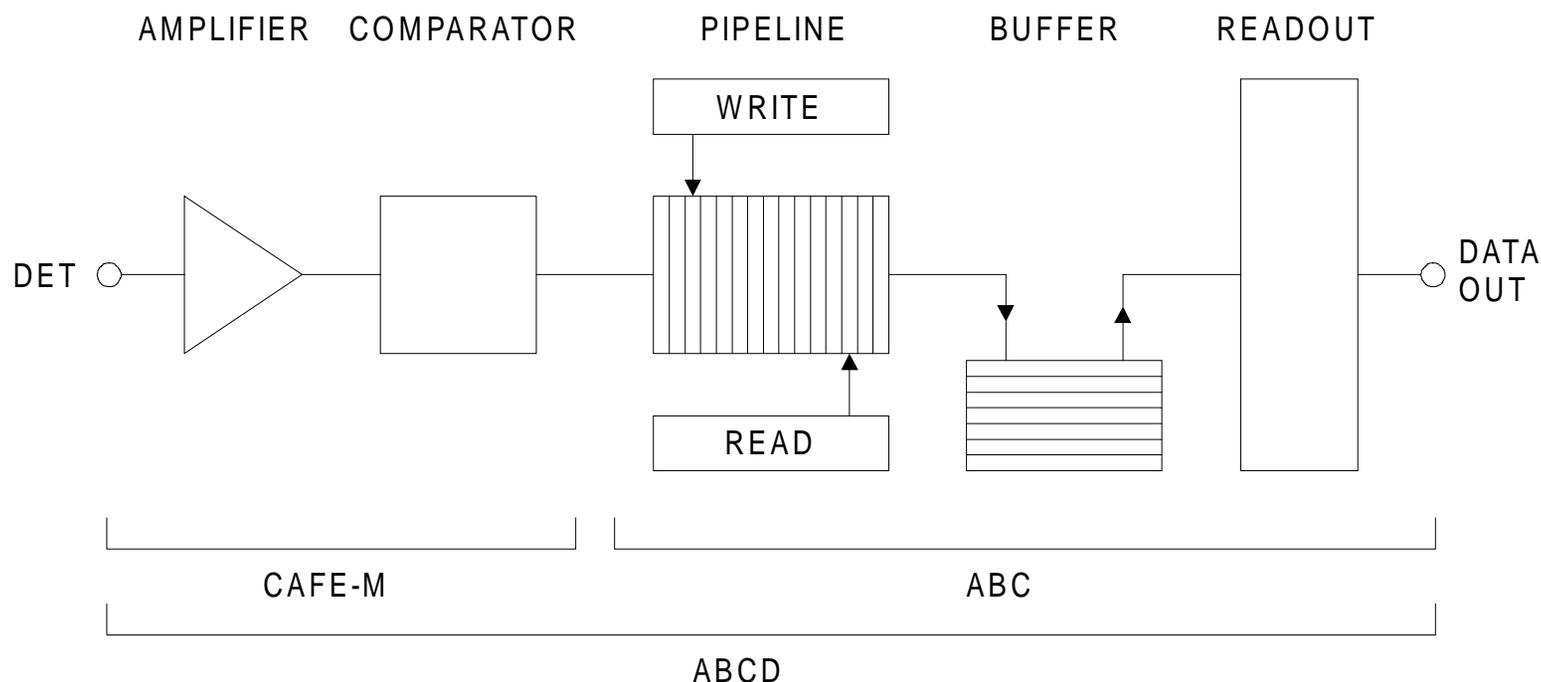
WBS 1.1.2 Silicon Strip System

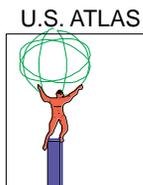
- **Scope**
 - ◆ No changes
- **Schedule**
 - ◆ US schedule and current ATLAS schedule(not baselined by ATLAS) now in reasonable agreement(see comparison later). Both schedules were modified to reach consistency.
- **ETC Cost Model**
 - ◆ Major design choices made in last weeks -> reflected in revised electronics costs but not yet in hybrid or module costs. Will have to update.



WBS 1.1.2.1 Silicon Strip IC Electronics

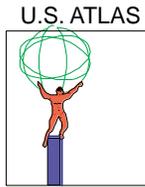
- Two rad-hard solutions were under development. Choice just made.
 - ◆ CAFÉ(bipolar from Maxim) + ABC(CMOS from Honeywell) - 2 chips.
 - ▲ This was the US cost baseline
 - ◆ ABCD(BiCMOS from Temic) - 1 chip.
 - ▲ This is now the baseline.





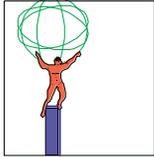
WBS 1.1.2.1 Silicon Strip IC Electronics

- Prototypes of all three ICs(CAFÉ, ABC and ABCD) were fabricated successfully and roughly on schedule last year.
- Both solutions, CAFÉ+ABC and ABCD, are functional pre-radiation with limited number of understood design errors(in ABC and ABCD). We have a preliminary but not final understanding of performance vs specifications via beam tests(at CERN and KEK) and laboratory measurements.
- The measured yields of CAFÉ/ABC are about as expected(roughly 70%) but the measured yield of ABCD is around 20%, about one-half that expected.
- The post-irradiation performance of the ABCD is superior to the CAFÉ.
- The contractual commitment from Temic is more advanced than for Honeywell.
- Taking all factors into account, the collaboration has chosen the ABCD.
- A design review of the ABCD is scheduled for next week at UC Santa Cruz.
- Successful completion of this design review will lead to a preproduction submission of 2 lots(40 wafers).

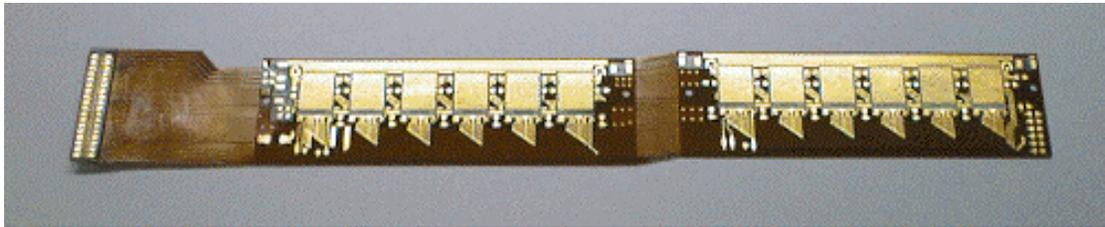


WBS 1.1.2.2 Silicon Strip Hybrids

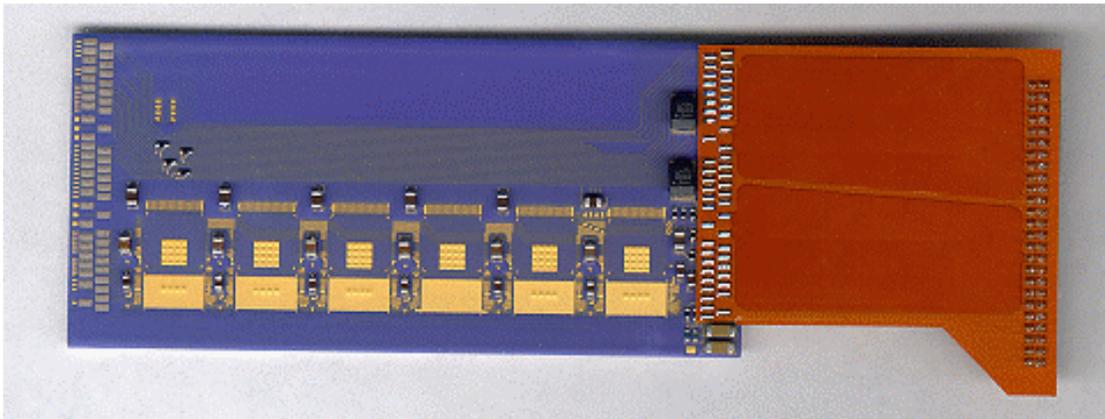
- Our baseline for barrel hybrids has been BeO hybrids and prototypes of these have been successfully manufactured and tested.
- ATLAS has considered alternative technologies: multi-layer kapton glued to a conducting(metallized carbon-carbon) mechanical support and direct deposition of traces on thermal pyrolytic graphite(TPG) - see next page.
- The collaboration has very recently selected kapton hybrids as the baseline, although some development of TPG may continue.
- We have in the last month obtained samples of the kapton hybrids and TPG hybrids for evaluation.
- The ETC has a revised cost for production of BeO hybrids that is slightly reduced compared to the FY97 baseline.
- We have not yet made an independent cost estimate of the kapton hybrids. Estimates made by ATLAS suggest that these would be cheaper than BeO but this remains to be verified according to US costing rules. This will take some months(until July) since we need experience and the US role in kapton hybrid fabrication is not settled.



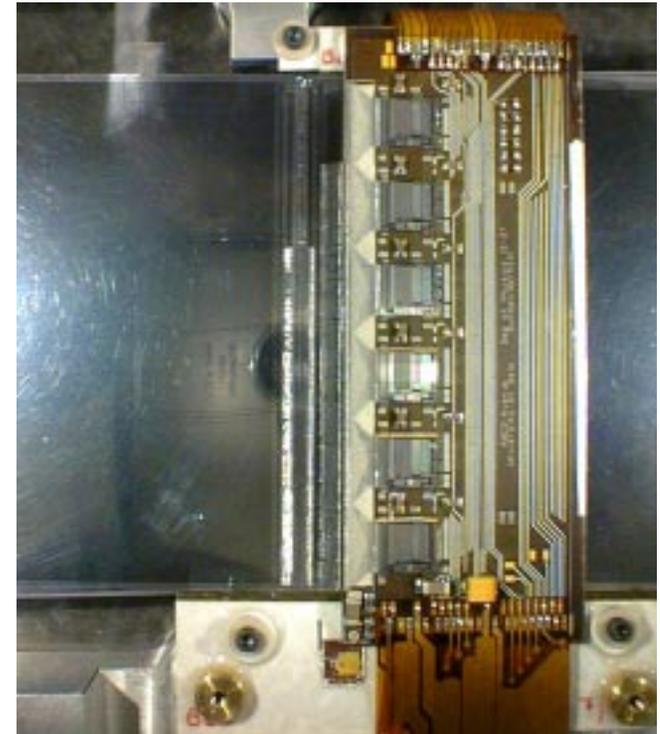
Silicon Strip Hybrids



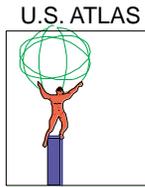
Copper on Kapton



Metal layers on beryllia

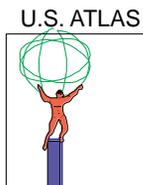


Metal layers/insulator
on pyrolytic graphite



WBS 1.1.2.3 Silicon Strip Modules

- **Tooling and procedures to make prototype modules in place and operational.**
- **Clean space available for production assembly.**
- **Most of effort on modules has been to study electronics and hybrids.**
- **Are at early stage in this process(as expected from our schedule).**
- **But need soon more ATLAS-wide attention and review of preparations of assembly sites(including US) and coordination of delivery of components to ensure effective preproduction startup by end this year.**



WBS 1.1.2 ETC

1.1.2.1 IC Electronics

- ◆ Preproduction fabrication cost based on measured yield(20%)
- ◆ Production costs based on minimum yield guaranteed by vendor(26%)
- ◆ Costs based on firm quotes from agreed Frame Contract with CERN and Temic that fix costs/wafer through end of 2003.
- ◆ Have added systems engineering support well into module production
- ◆ Have added administrative support to help track rad-hard ICs(controlled objects) that must be rigorously accounted.

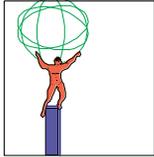
1.1.2.2 Hybrids/Cables

- ◆ Current estimate based on revised quotes for BeO hybrids.
- ◆ No longer valid given very recent choice by collaboration. Need until July to update.

1.1.2.3 Modules

- ◆ Revised fabrication costs for thermal baseboards and related assembly
- ◆ Added some assembly equipment(glue dispense robot)
- ◆ Labor estimate largely unchanged - need more experience before updating(by November)

				TPC	
	Baseline	ETC	Actuals	ETC+Actuals	Delta
WBS	FY00 \$K	FY00\$K	\$K	\$K	\$K
1.1.2	5698	4824	911	5735	(37)

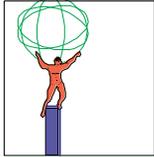


WBS 1.1.2 Milestones

ATLAS Milestones	Current ATLAS*	Baseline US	Forecast US
SCT Front end electronics			
Decision on vendor	2/15/00	12/10/99	2/28/00
Final design review	3/6/00	3/3/00	3/6/00
Front end electronics order placed (5% + 95%)	4/28/00	3/31/00	5/1/00
Front end electronics PRR	10/20/00	3/2/01	2/12/01
<i>Release order for main production (95%)</i>	<i>2/16/01</i>	<i>3/30/01</i>	<i>3/5/01</i>
Front end electronics 10% available	7/6/01	9/11/01	8/15/01
Front end electronics 25% available	9/14/01	11/22/01	10/26/01
Front end electronics production complete	8/2/02	11/21/02	8/19/02
SCT Barrel module hybrids assembly			
Hybrid choice decision	2/5/00	12/10/99	2/5/00
Final design review	4/10/00	2/11/00	5/10/00
Hybrid order placed (5% + 95%)	7/10/00	2/28/00	5/25/00
Hybrids PRR	2/16/01	4/11/01	2/15/01
Release order for main production (95%)	3/2/01	6/6/01	3/15/01
10% hybrid assembly available	10/19/01	1/15/02	8/1/01
25% hybrid assembly available	1/18/02	3/26/02	10/24/01
Barrel hybrid assembly complete	11/22/02	3/14/03	11/21/02
SCT Barrel module tooling			
Assembly tooling review	4/7/00	11/10/00	11/1/00
Tooling ready for production of modules	1/26/01	11/13/00	11/2/00
Module PRR	3/5/01	4/11/01	3/6/01
SCT Barrel modules			
Order placed silicon barrel modules (5% + 95%)	4/16/01	11/13/00	11/1/00
<i>Release order for main production</i>	<i>9/17/01</i>	<i>6/5/01</i>	<i>4/3/01</i>
Barrel silicon module 10% complete	1/7/02	11/20/01	9/18/01
Barrel silicon module 25% complete	4/15/02	2/26/02	12/25/01
<i>Barrel silicon modules complete</i>	<i>4/14/03</i>	<i>8/26/03</i>	<i>4/11/03</i>
* Current ATLAS schedule not baselined			
<i>Level 2 US milestones</i>			

Needs revision

Needs review



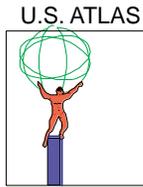
Risks and Issues

- **Risks**

- ◆ Reliability and stability of Temic (in principle solved by Frame Contract that guarantees minimum yield and specifies production through 2003) -> go fast. In principle, CAFE/ABC is backup or deep submicron, but either would introduce delay(year+).
- ◆ Find IC problems that require lengthy redesign after launching preproduction submission in next few months -> not much, live with or take schedule hit.
- ◆ Low dose rate effect on IC bipolar front-ends -> setting up more tests but these take long time
- ◆ Limited experience with kapton hybrids in silicon strip systems -> go fast
- ◆ Electronics/hybrid tests, system tests will indicate substantial changes to module assembly procedures -> do these tests as fast as possible, multi-module systems tests this summer.
- ◆ Continued need for resources to understand electronics performance will slow down preparations for module production -> decouple the electronics issues from proceeding with mechanical activity lead to production to extent possible - more technical manpower(expected from base support).

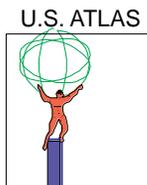
- **Issues**

- ◆ Inability of US to influence production schedule. Have had very little role in ABCD design, most module parts(hybrids, baseboards, detectors) now come from outside US with no US direction.
- ◆ Life-time buy and spares for ICs and other critical components.



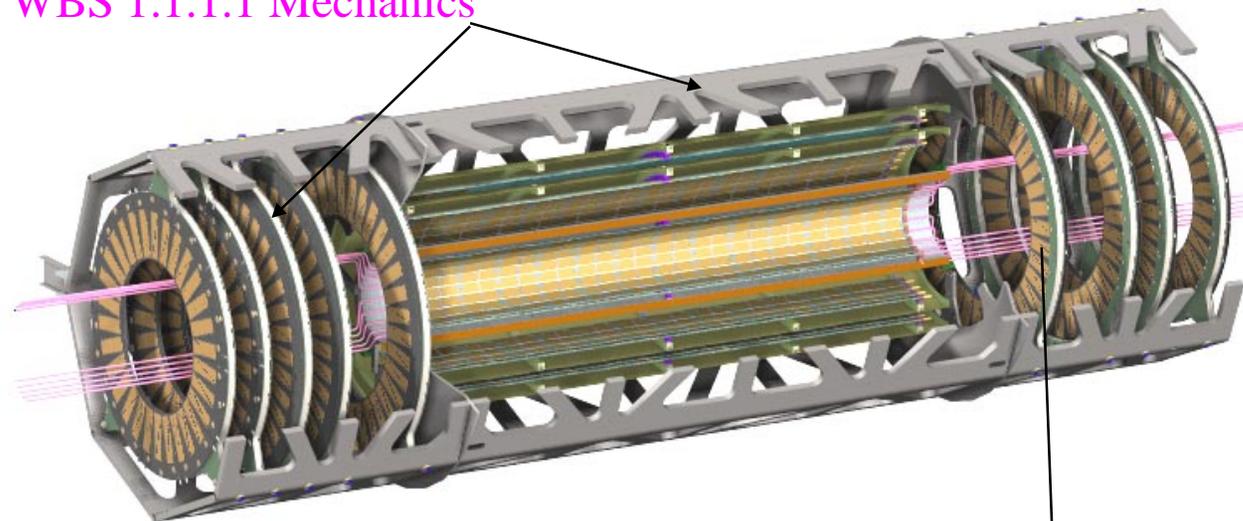
WBS 1.1.1 Pixel Project Status

- Approved October 1998 for development through FY2000 with fixed project support - so-called Pre-Technical Baseline.
- Review in summer 2000 leading to construction baseline - this is still our plan but the review date will slip from May 00 by 3-4 months until near end of FY00.
- Proceeding with this baseline review is critical to meet ATLAS schedule and we will be ready with the appropriate detailed cost and schedule estimates.
- Two internal reviews were planned before baseline review
 - ◆ March 1999 complete.
 - ◆ This review in next few days counts as the second review.
 - ◆ In addition, have added mechanics review in April that will also cover mechanical aspects of module assembly.



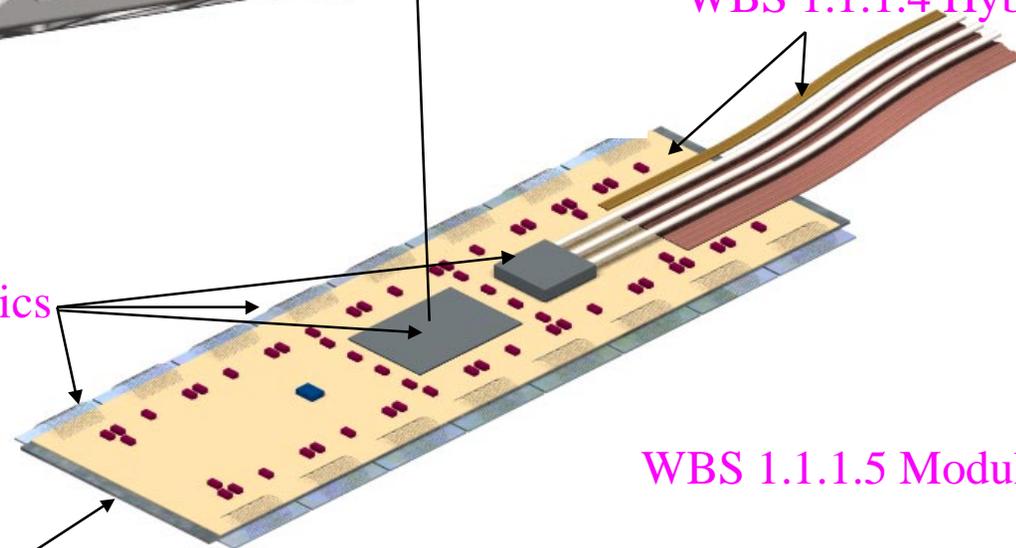
WBS 1.1.1 Pixel System

WBS 1.1.1.1 Mechanics



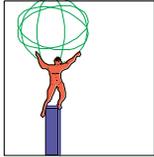
WBS 1.1.1.4 Hybrids

WBS 1.1.1.3 Electronics



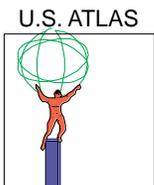
WBS 1.1.1.5 Modules

WBS 1.1.1.2 Sensors



WBS 1.1.1 Technical Status Summary

- **1.1.1.1 Mechanics**
 - ◆ Prototypes of major elements fabricated and under test. Looks good so far.
 - ◆ Major technical issues: cooling system uncertainty(non - US responsibility but affects our design) and cable plant lack of design/cost(we have picked up most of this for now to advance project and control interfaces).
- **1.1.1.2 Sensors**
 - ◆ Round 1, round 1.5 prototype sensors fabricated and tested successfully. Round 2 prototypes just returned and under test. Final Design Review completed on Dec. 3. PRR on Feb. 2 complete.
 - ◆ Major technical issue:testing after irradiation and production yield
- **1.1.1.3 Electronics**
 - ◆ Full-scale, rad-soft prototype tests very successful. Proof-of principle - it can work.
 - ◆ First rad-hard fabrication complete(Temic). Design errors identified but major problem is believed to be very low yield. Honeywell design underway, but substantially late.
 - ◆ Major technical issue: Combination of design flaws and low yield likely to prevent meaningful irradiation testing until after refabrication of Temic chip.
- **1.1.1.4 Hybrids**
 - ◆ Prototype flex hybrids successfully manufactured by two sources. Few modules built, design looks OK
 - ◆ Major technical issues: detailed design verification with multiple modules and production preparations.
- **1.1.1.5 Modules**
 - ◆ Prototypes fabricated and tested but not enough built to understand systems aspects.
 - ◆ Critical bump bonding under control with limited outstanding issues with two vendors, third vendor being qualified by ATLAS.
 - ◆ Major technical issues: yield of assembly process and radiation testing

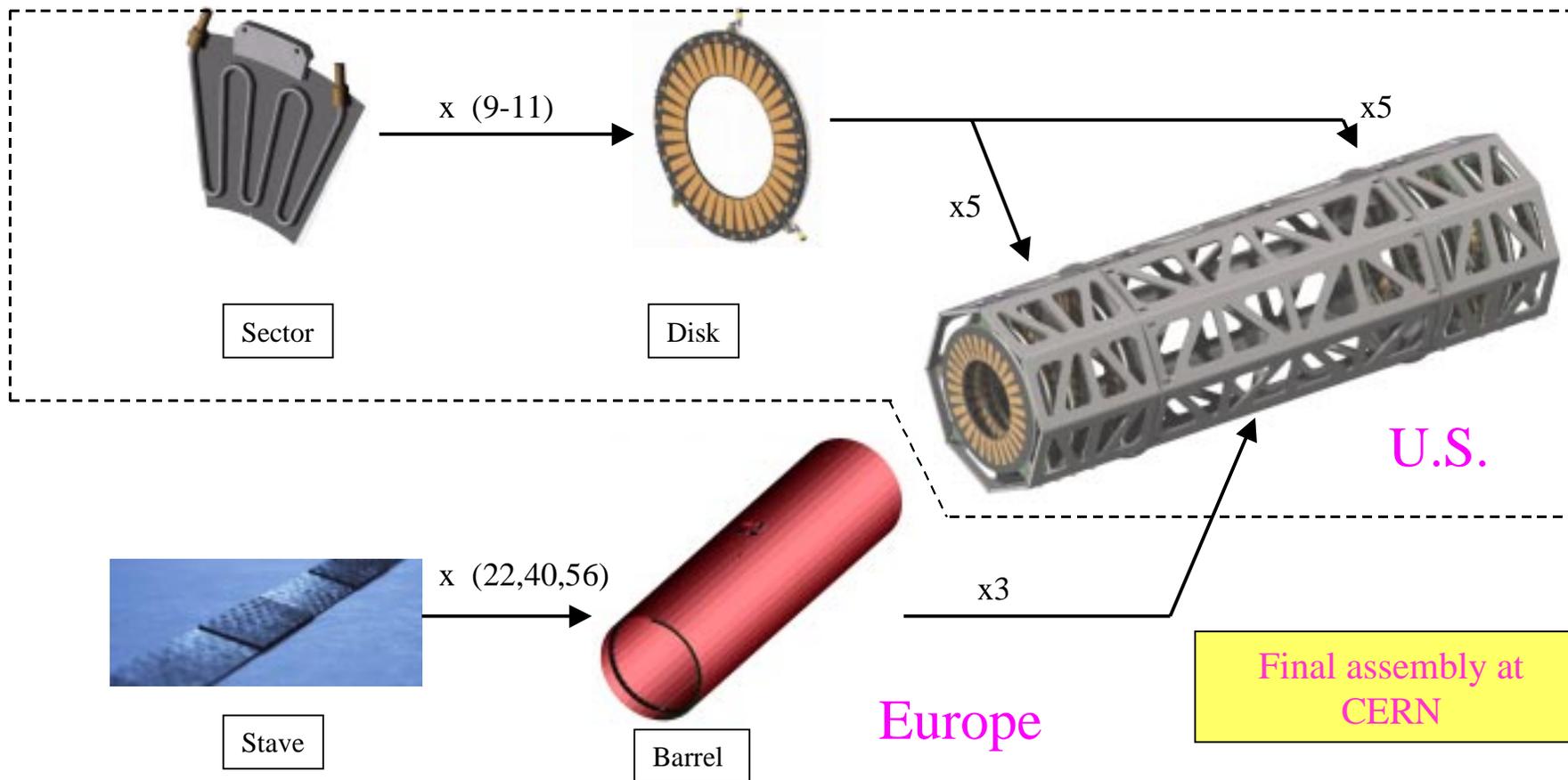


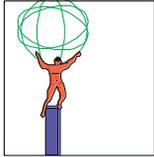
WBS 1.1.1.1 Pixel Mechanics

Local support structure

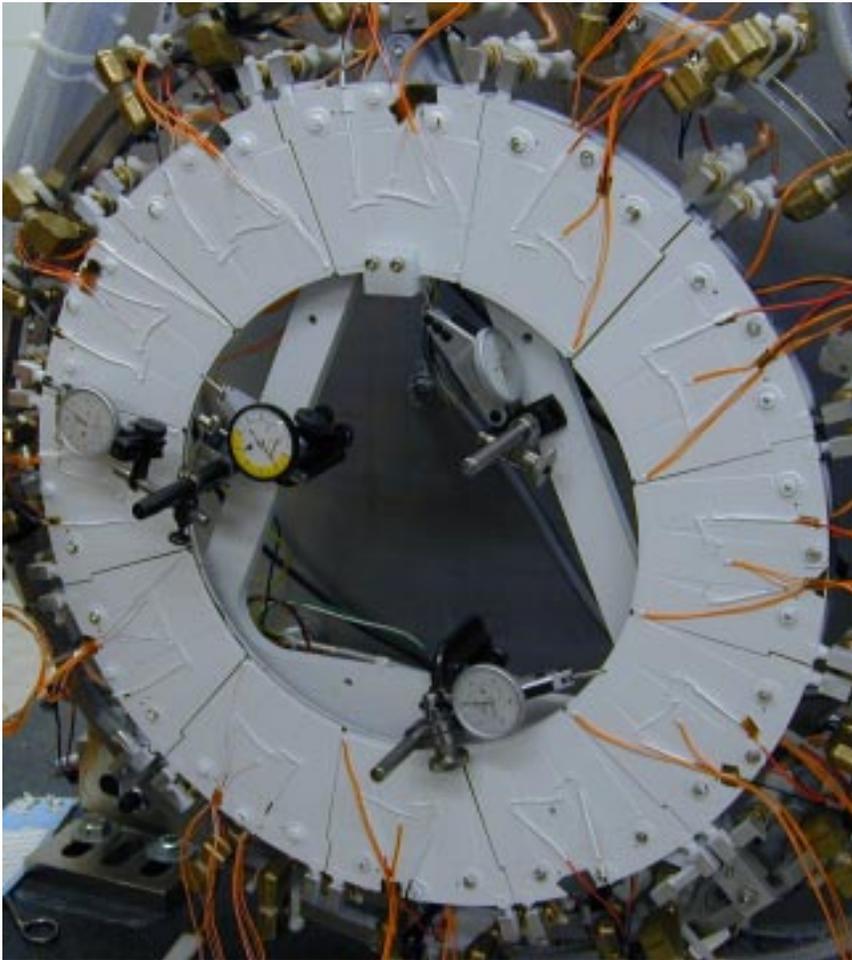
Intermediate support structure

Global support structure

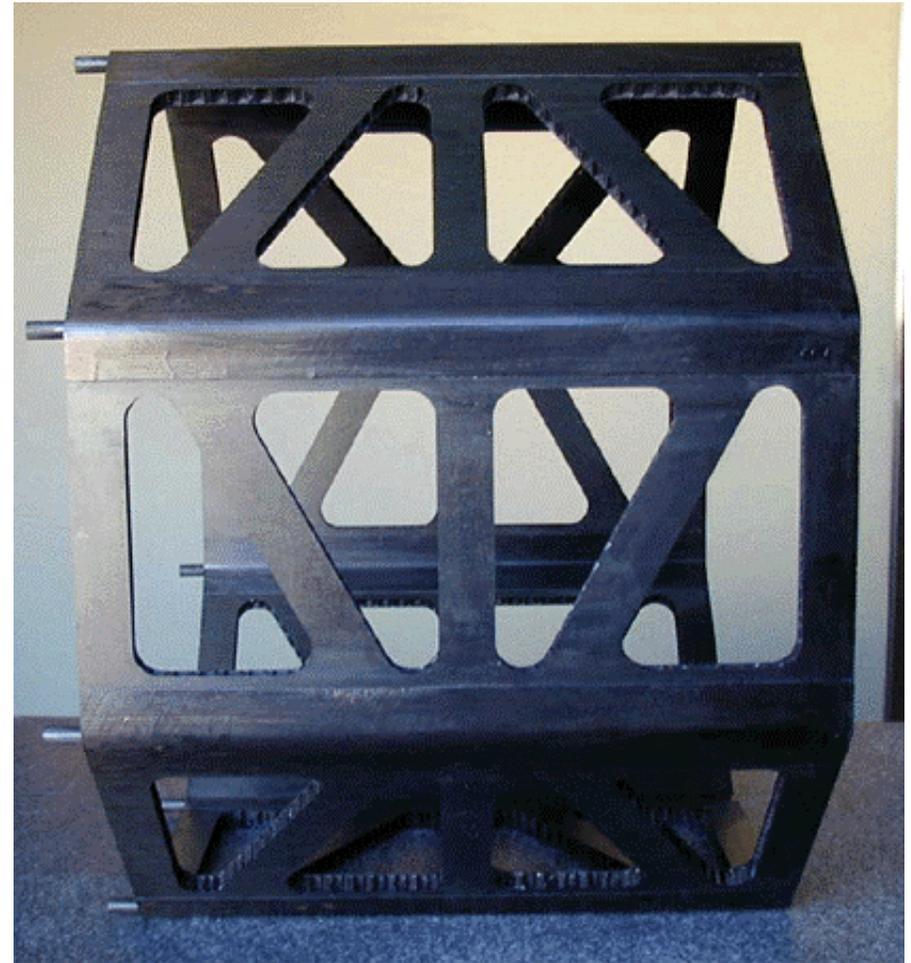




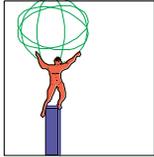
WBS 1.1.1.1 Prototypes



Prototype disk

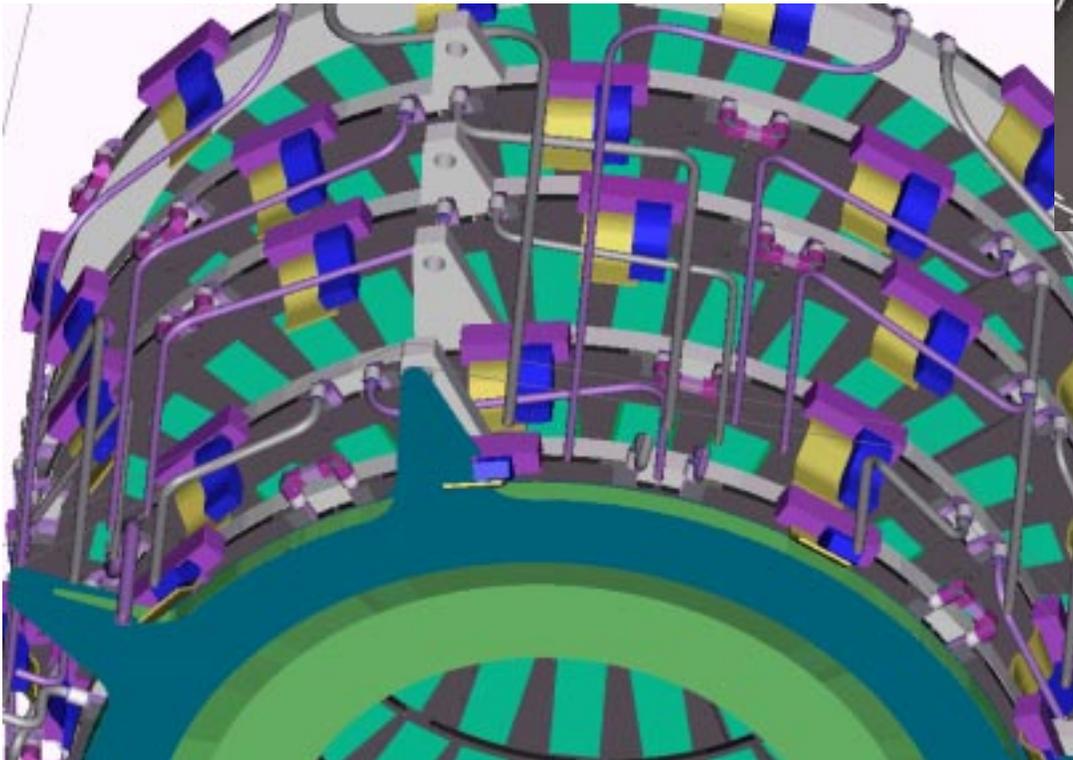
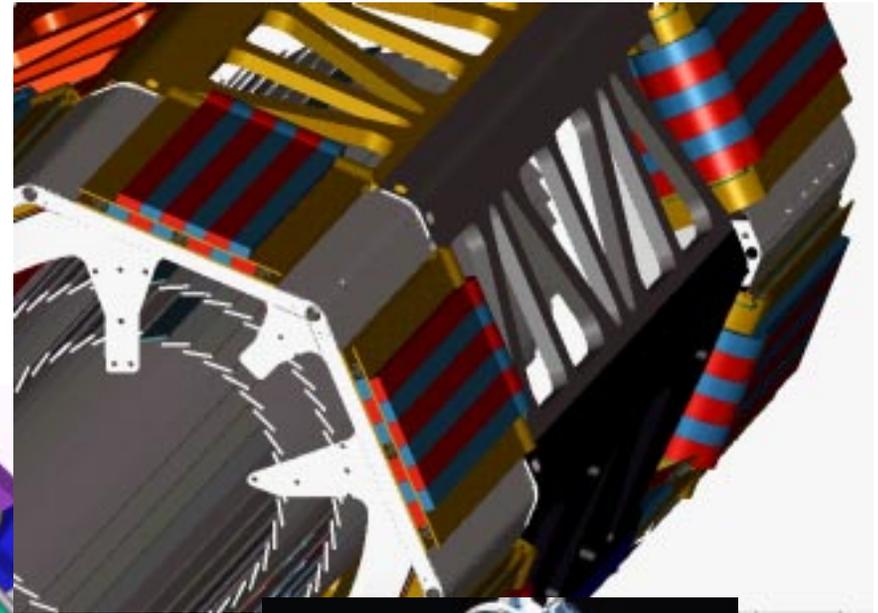


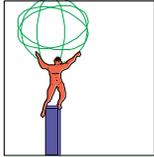
Prototype end frame



WBS 1.1.1.1 Prototypes/Design

- Cable and coolant pipe plant is major design issue for U.S. deliverables.
- Successful effort in last few months to bring this under control.





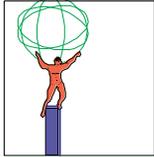
WBS 1.1.1.1 Risks and Issues

- **Risks**

- ◆ Cooling history. Binary ice -> liquid or evaporative fluorinerts -> low pressure(4-5 bar) evaporative -> high pressure(up to 10 bar) evaporative ->???. What to do? Conservative approach for design - decouple from cooling situation.
- ◆ Costly cable plant -> do design and control interfaces.

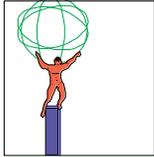
- **Issues**

- ◆ Will be ready to proceed with construction design for some items in about mid this FY. These funds were not included in Development budget -> have schedule design review April 10 as part of week long pixel mechanics meeting -> success => advanced construction funding.
- ◆ Because of cooling gyrations, need more Development funds for new baseline sector. Also some for cable plant mockup and prototypes, not foreseen when Development budget set. Again review in April.



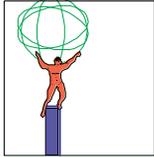
WBS 1.1.1.2 Pixel Sensors

- **Prototype 1.0 and 1.5 sensors fabricated and tested extensively, including with rad-soft electronics. A few irradiated sensors bonded to rad-soft electronics - work after lifetime fluence.**
- **Final Design Review completed on December 3, 1999.**
- **Production Readiness Review completed on February 2, 2000.**
- **Recent results on oxygenated silicon increase substantially radiation resistance and pixels will use this advantage.**
- **Risks**
 - ◆ **Lack of irradiation testing before starting preproduction -> these tests are planned over next months.**
 - ◆ **Formally qualified vendors have limited capacity and will take some time for production -> which is why preproduction is scheduled this FY. But need to balance against item above.**
- **Issues**
 - ◆ **None**



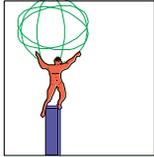
WBS 1.1.1.3 Pixel Electronics

- Full-scale prototypes(FE-A, FE-B and FE-C) fabricated in rad-soft technologies in 1998 and tested extensively in 1998 and 1999.
- Can't do justice to all of these impressive data.
- Bottom line - proof-of-principle demonstrated.
- Rad-hard design choices assuming working chips
 - ◆ DMILL(Temic) for outer layers(90%) -> lower cost, availability of design rules.
 - ◆ Honeywell Sol for innermost layer(10%) -> higher granularity(smaller pixel size) possible, believed to be more radiation hard. Installed much later than outer layers.
 - ◆ This strategy keeps two vendors going in phased way.
- Third alternative is deep submicron(0.25μ) process, which has had some recent success outside ATLAS. No work ongoing in ATLAS at this time - lack of manpower.

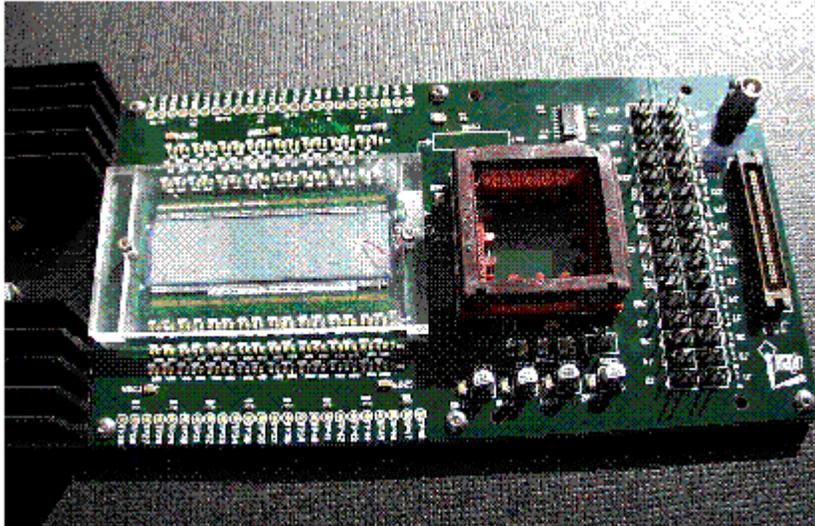


WBS 1.1.1.3 Pixel Electronics

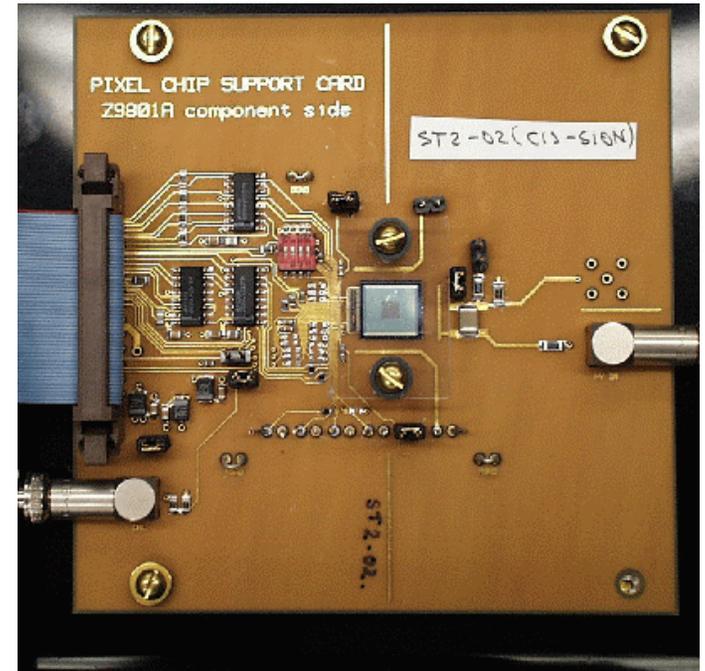
- **First rad-hard prototype(FE-D from Temic) delivered in October '99**
 - ◆ Essential functionality of design has been largely verified but
 - ◆ A number of design errors made as verified by simulation and/or measurements.
 - ◆ And inadequate design rule checking by the vendor
 - ◆ Remaining problems are attributable to processing problems and these result in very low yield for fully functional chips
 - ◆ Detailed testing to understand yield problem underway. This includes assemblies with detectors.
 - ◆ Backup run by vendor under way for delivery in mid-March
 - ◆ Design modifications can be made for next submission by about end-March, but will await results from backup run and additional testing and simulation before resubmission.
- **Honeywell design progressing**
 - ◆ Slowed down by inability to get design rules(State Dept. approval) to European designers (just solved) and by need to devote more resources to DMILL chip.
 - ◆ Nevertheless design is advancing, additional designer familiar with project hired in US by next month and hope for submission mid-year, giving chips by end year.



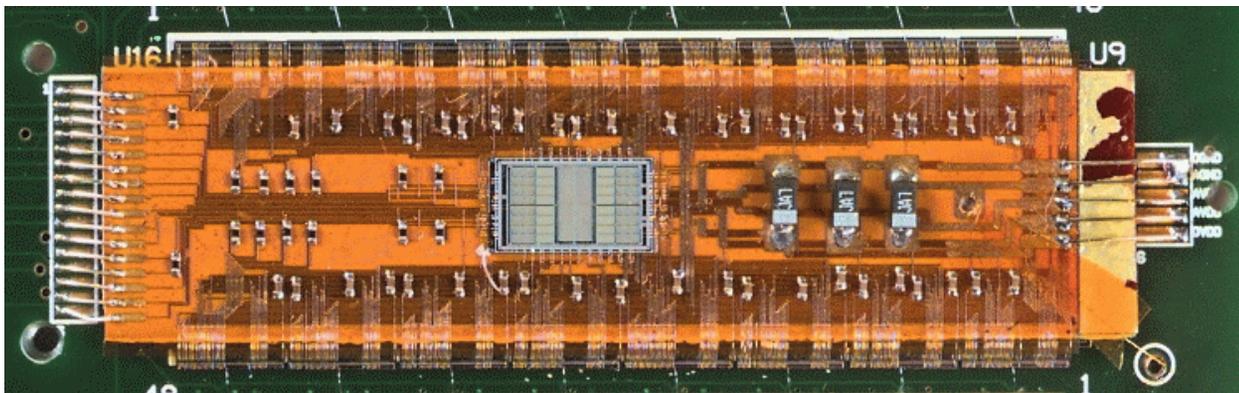
What Has Been Tested



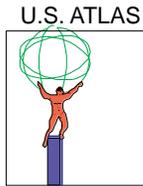
Bare 16-chip modules



Dozens of single chip/sensor assemblies of different types



16-chip modules with flex hybrid



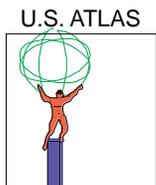
WBS 1.1.1.3 Risks and Issues

- **Risks**

- ◆ This is the cost and schedule risk for the Pixel Project.
- ◆ Technical risks: radiation hardness and basic ability of vendors.
- ◆ Cost risk(lower Temic yield or using HSOI for entire project) currently covered by large contingency (100% or about \$1M) in ETC draft but US contributes about 20% of total cost.
- ◆ Schedule risk: too many iterations needed to achieve good yield and performance.

- **Issue**

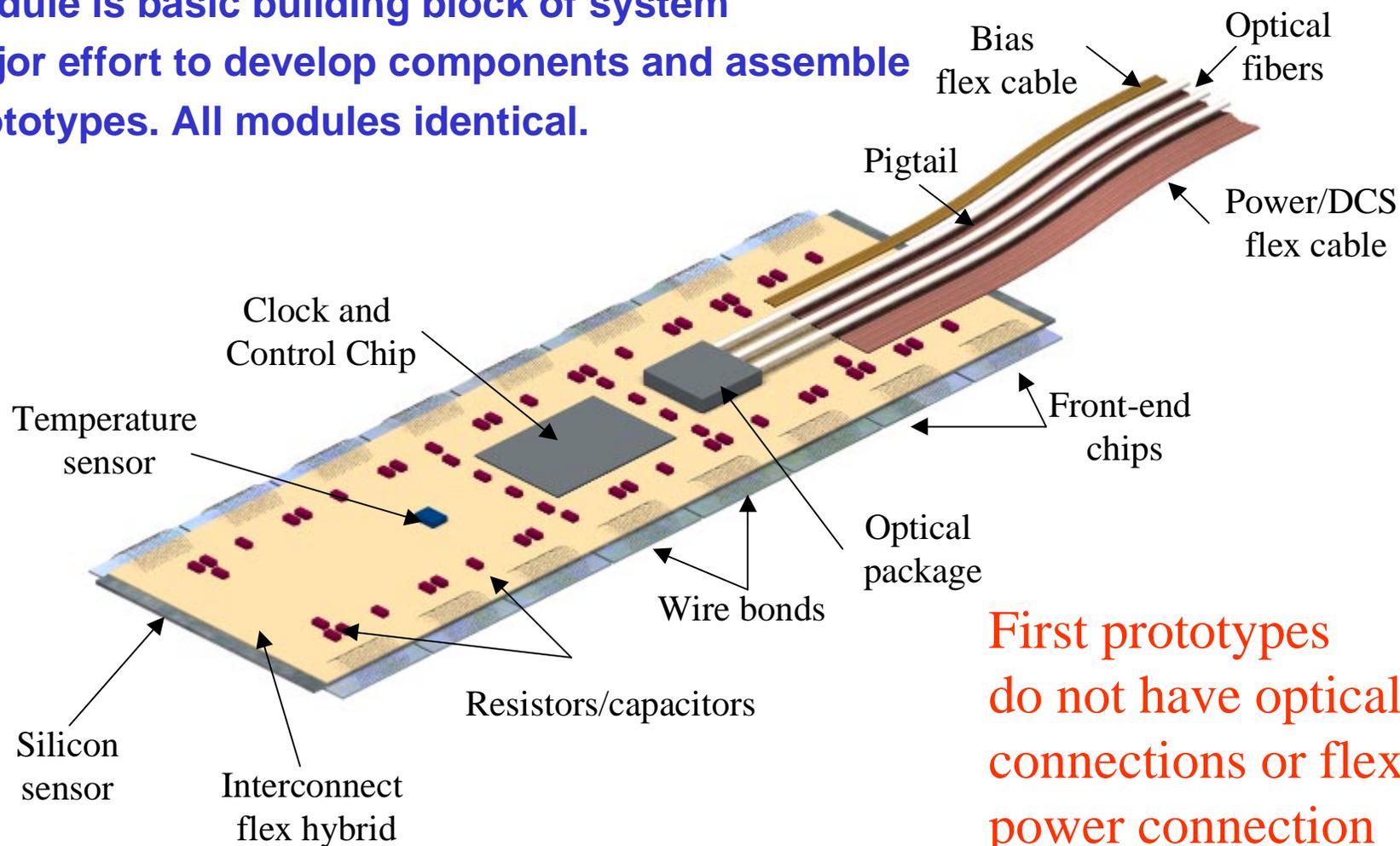
- ◆ The only way to advance the schedule is with more manpower for IC design and testing. We have been trying and are trying to do this, with some recent success.
- ◆ To speed up more or to begin deep submicron development for pixels in the US in the next year will require more project money, if we can find the manpower.



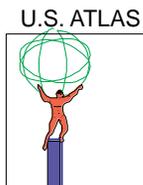
Pixel Module

Module is basic building block of system

Major effort to develop components and assemble prototypes. All modules identical.

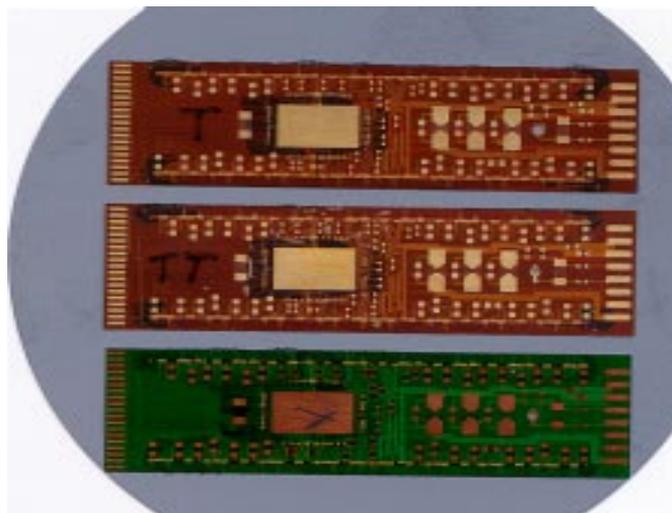


First prototypes do not have optical connections or flex power connection



WBS 1.1.1.4 Pixel Hybrids

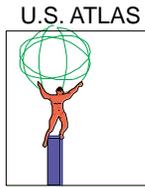
- Flex hybrids v1.x manufactured at CERN(two generations) and most recently by US company(Compunetics).
- Design of v2.x launched and ready to begin fabrication shortly.
- Design of flex hybrid 100% responsibility of Oklahoma. Pigtail designs separated out: barrel in Europe and disk in US(UOK/LBL).
- Risks
 - ◆ Need more experience(electronics limited)
 - ◆ Vendor yield
- Issues
 - ◆ None



CERN - first version

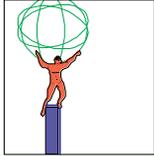
CERN - second version

Compunetics

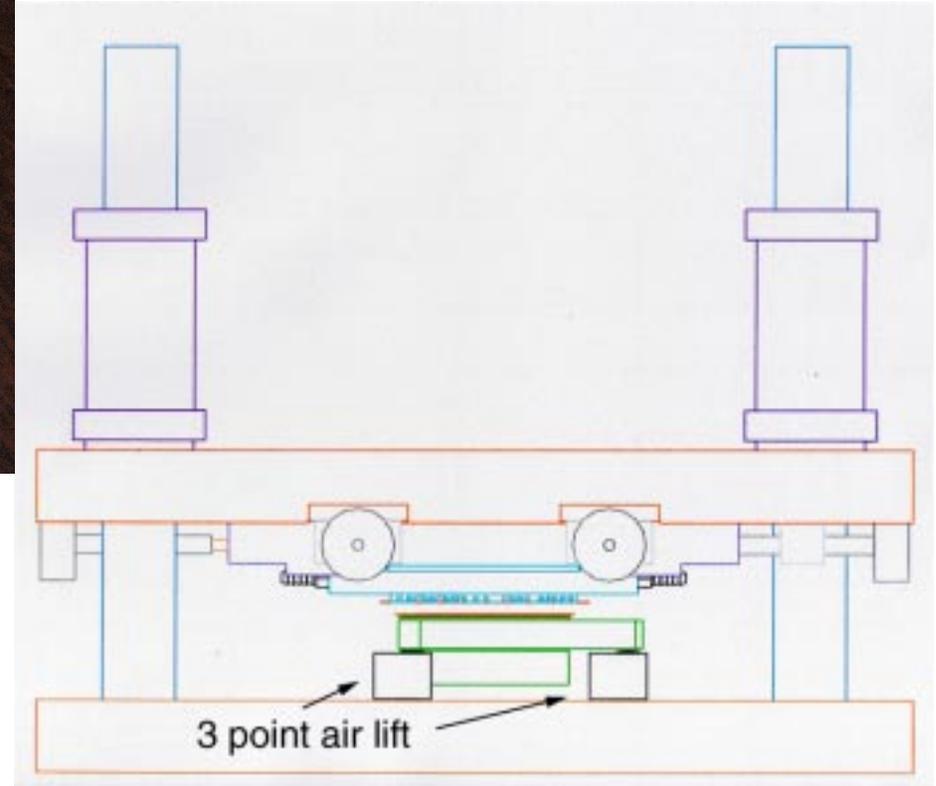
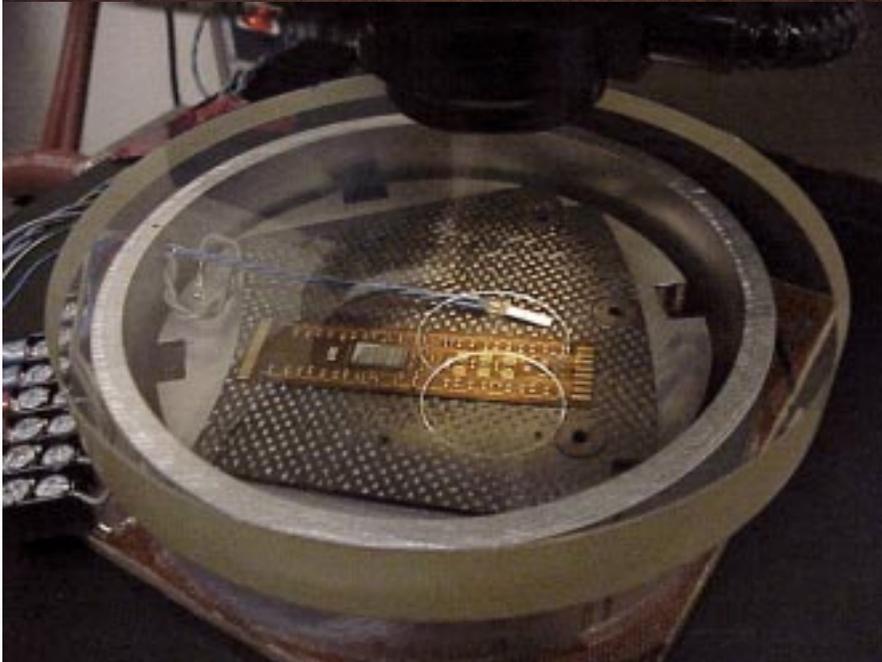
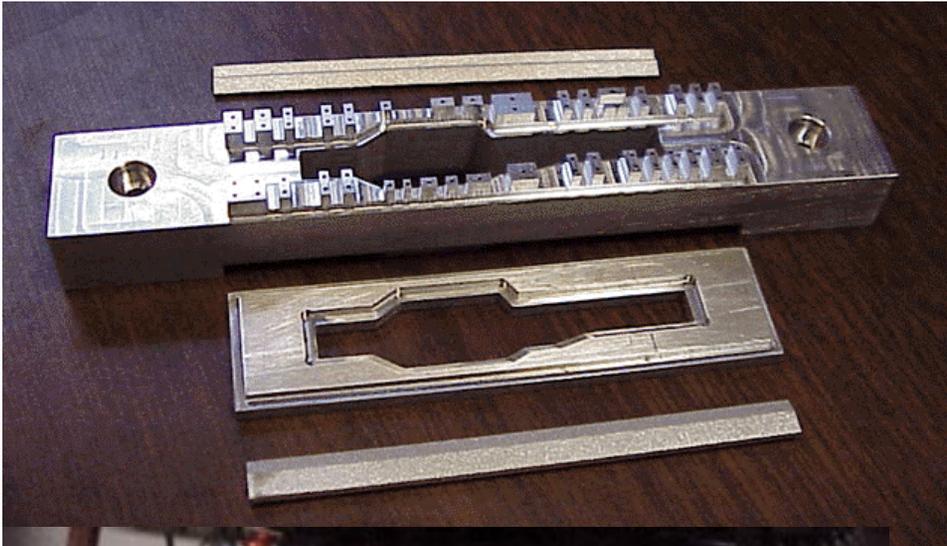


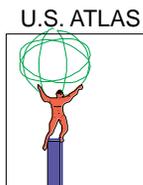
WBS 1.1.1.5 Pixel Modules

- Modules include wafer thinning, dicing, bump bonding of ICs to sensor, attachment of flex to “bare module” and attachment of pigtailed and wire bonding and attachment of modules to mechanical support.
- Bump bonding status
 - ◆ Two vendors in Europe have demonstrated acceptable mechanical yield (low defect rate) and third European vendor started. Keep touch with CMS/B-Tev, who are working with different vendors.
 - ◆ US role much reduced and we have dropped production responsibility, except perhaps for wafer thinning (only successes so far in US) and perhaps some X-ray inspection (Italian vendor currently lacks this capability).
- Conceptual design of module attachment procedures and tooling completed in US. Prototype tooling started.
- Currently working on mechanical properties, wire bonding tests, gluing tests, irradiation, etc.
- Risks
 - ◆ Yield -> practice, practice and then practice some more. Dummy program underway.
- Issues
 - ◆ None



WBS 1.1.1.5 Pixel Modules

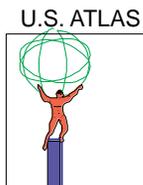




WBS 1.1.1 Scope and ETC

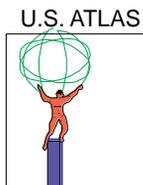
- The ETC has two parts. Completion of the Pre-Technical Baseline and a “rough draft” of proposed production.
- Pre-Technical Baseline
 - ◆ **Mechanics:** increase in structure prototypes and services(prototypes and mockup) -review in April before BCP made
 - ◆ **Sensors:** no change(after BCPs for advancing preproduction and for engineering manpower)
 - ◆ **Electronics:** no change assuming no deep submicron and no new manpower
 - ◆ **Hybrids:** increase in design and prototypes. Also review about April before BCP made.
 - ◆ **Modules:** no change

				TPC	
	Baseline	ETC	Actuals	ETC+Actuals	Delta
WBS	FY00 \$K	FY00\$K	\$K	\$K	\$K
1.1.1	2347	1504	1005	2509	(162)



WBS 1.1.1 Deliverables - Draft Production ETC

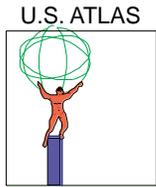
- **Mechanics**
 - ◆ Disks, frame and cones.
 - ◆ Thermal barriers(now part of frame) and integrated B-layer insertion rails
 - ◆ Contribution to final assembly at CERN
 - ◆ Cable plant inside ID volume.
- **Sensors**
 - ◆ Silicon wafers(about 20% of total) and testing of same
- **Electronics**
 - ◆ Wafers for outer layers and wafers for B-layer(about 20% of total in each case)
 - ◆ Testing of about one-half of all wafers
 - ◆ One-half of wafers(few) for optical electronics
- **Hybrids**
 - ◆ All module flex hybrids and all disk pigtails
 - ◆ Currently loading of all of these but under discussion.
- **Modules**
 - ◆ Assembly of all disk modules and attachment to disk structures and testing.
 - ◆ Currently all front-end IC wafer thinning, dicing but under discussion.
 - ◆ X-ray inspection of about one-half of bare modules but also under discussion.
- Compared to guesses in 1996-97, mechanics has increased, sensors and electronics the same, hybrids+modules same, but have focussed on hybrids and dropped bump bonding.
- Current draft estimate base cost fits within allocation(\$7.2M) outside baseline.



WBS 1.1.1 Pre-Technical Baseline Milestones

Milestone	Current		Comments
	Baseline	Forecast	
Production Baseline Review	5/29/00	9/10/00	
Mechanics			
Disk sector PRR	5/3/00	9/29/00	
Global support FDR	2/2/01	9/29/00	
Sensors			
Sensor FDR	1/20/00	12/3/99	
Begin preproduction fab	7/20/00	7/20/00	
IC Electronics			
Complete fab DMILL prototype	7/23/99	10/25/99	
Complete fab Honeywell prototype	8/25/99	12/15/00	Now only B-layer
IC vendor selection	2/29/00	DONE	Assuming DMILL has acceptable yield
Complete fab 2nd rad-hard prototype	11/29/00	7/1/00	
Hybrids			
Select production vendors	2/8/00	2/15/01	
Modules			
Select module production vendors(bump bonding)	4/3/00	1/10/01	But will be sole source orders

Production schedule under development. Critical path will be IC electronics - moving from prototypes to preproduction and then production.



Institutional Responsibilities

ALB LBL ISU UCSC UNM UOK UW OSU

1.1.1 Pixels

1.1.1.1 Mechanics

X

X

1.1.1.2 Sensors

X

X

X

1.1.1.3 Electronics

X

X

1.1.1.4 Hybrids

X

X

X

1.1.1.5 Modules

X

X

X

X

X

X

1.1.2 Silicon Strips

1.1.2.1 IC Electronics

X

X

1.1.2.2 Hybrids

X

X

1.1.2.3 Modules

X

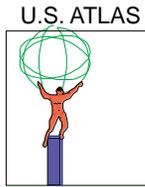
X

1.1.3 RODs

X

X

X Change since last review



WBS 1.1 Summary

- **1.1.1 Pixels**
 - ◆ Technical progress continues to be excellent, although we could have been luckier on the rad-hard electronics.
 - ◆ Electronics schedule is the critical issue.
 - ◆ Baseline review by end FY00 - needed to maintain ATLAS schedule - is planned.
- **1.1.2 Silicon Strips**
 - ◆ 2nd generation IC prototypes fabricated on schedule.
 - ◆ Choice of IC design made. Hybrid choice made.
 - ◆ Preproduction IC submission forecast +1 month relative to baseline.
 - ◆ Rest of project driven by electronics(at present).
- **1.1.3 Read-Out Drivers(ROD)**
 - ◆ Design team in place.
 - ◆ Prototype design advancing well